**Amendments to the Claims**:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Withdrawn) A thin film transistor type display device, comprising:

a first substrate;

a second substrate;

thin film transistors formed on the first substrate;

wiring lines formed on the second substrate; and

an element chip including at least one of the thin film transistors peeled off from the first substrate and transferred to the second substrate, holographic lithography being used in patterning of the thin film transistors.

2. (Withdrawn) A thin film transistor type display device, comprising:

a first substrate;

a second substrate;

thin film transistors formed on the first substrate;

wiring lines formed on the second substrate; and

an element chip including at least one of the thin film transistors peeled off from the first substrate and transferred to the second substrate, dynamic auto focus system being used in patterning of the thin film transistors.

3. (Withdrawn) The thin film transistor type display device according to Claim 1,

a design rule of 1.0 μm or less being used in the patterning of the thin film transistors.

4. (Withdrawn) The thin film transistor type display device according to Claim 1,

only a polycrystalline silicon layer and a first metal layer being used as the wiring lines of the element chip.

5-6. (Canceled)

7. (Withdrawn) A thin film transistor circuit board, comprising:

thin film transistors manufactured by the method of manufacturing the thin film elements according to Claim 6.

8. (Withdrawn) An electro-optical device, comprising:

the thin film transistor circuit board according to Claim 7.

9. (Withdrawn) An electronic apparatus, comprising:

the electro-optical device according to Claim 8.

10.-11. (Canceled)

12. (New) A method of manufacturing a thin film transistor circuit substrate, comprising the steps of:

forming a plurality of element chips, each having at least one thin film transistor, on a first substrate via a peeling layer;

forming a wiring line on a second substrate;

pressingly attaching at least one element chip of the plurality of element chips in a predetermined position of the second substrate via adhesive, and electrically connecting the at least one element chip and the wiring line; and

peeling the at least one element chip from the first substrate, by irradiating a laser beam onto the peeling layer, after electrically connecting the at least one element chip and the wiring line;

wherein the step of forming the thin film transistor includes the steps of forming an amorphous silicon layer on the peeling layer, crystallizing the amorphous silicon layer by irradiating a laser beam thereonto, and then forming a polycrystalline silicone layer by

patterning the crystallized amorphous silicon layer, forming an insulating film on the first substrate and the polycrystalline silicon layer, and forming the gate metal on the insulating film, and then forming a gate electrode by patterning the gate metal; wherein

holographic lithography and a follow focus system are used for patterning the amorphous silicon layer and the gate metal;

stepper exposure is used for patterning other than patterning the amorphous silicon layer and the gate metal; and

a design rule finer than a design rule used for the other patterning is used for patterning the amorphous silicon layer and the gate metal.

13. (New) The method according to claim 12, further comprising using the design rule of 1.0 micron or less for the patternings.

14. (New) The method according to claim 12, the other patterning including the patterning of the crystallized amorphous silicon layer.